REMARKS/ARGUMENTS

Reconsideration of the application is respectfully requested for the following reasons:

Claim 1 is objected to because two typographical errors according to the detailed action. One is in line 6 of claim 1, wherein "polysilicon" is misspelled as "polysilicen". The other one is in line 8 of claim 1, wherein "said" is mistyped as "Said". However, Applicant has not found such errors in both Applicant's own version and the publication version on the USPTO(US 2004/0048482) of the application. Nevertheless, Applicant amends claim 1 as well as claim 7 to replace "polysilicen/polysilicon" with "conductive".

Rejection of Claims 1-12 Under 35 U.S.C. § 112, second paragraph

In respond to this rejection, Applicants have amended claims 1 and 7 to replace "polysilicen/polysilicon" with "conductive". Reconsideration of claims 1-12 is respectfully requested.

Rejection of Claims 1 and 3-6 Under 35 U.S.C. §102(e)

Claims 1 and 3-6 are rejected under 35 U.S.C. §102(e) as being anticipated by Hsieh (US 6,326,263).

Applicants respectfully traverse this rejection. This rejection is traversed because Hsieh actually fails to teach every element of the claimed invention. According to MPEP §2131, To Anticipate A Claim,

The Reference Must Teach Every Element Of The Claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

Particularly, Hsieh discloses a method of fabricating a flash memory cell having a self-aligned floating gate structure different to the claimed invention. For example, Hsieh teaches that a tunneling oxide layer 54 and a polysilicon layer 56 are formed on the silicon substrate 52. Then conventional lithographic and etching processes are used to define a predetermined pattern in the polysilicon layer 56, i.e. defined polysilicon layer 56 which is different to the claimed invention. After defining the polysilicon pattern, a defined sacrificial layer 58, which is made of silicon nitride, is formed on the semiconductor wafer 50 by means of conventional CVD process, lithographic and etching processes which is different to the claimed invention. The silicon substrate 52 is then etched using the sacrificial layer 58 which is not used in the claimed invention as a mask to form a shallow trench isolation (STI) pattern 64 on the silicon substrate 52.

Contrary to the teaching of Hsieh, the claimed invention patterns the first conductive layer, the tunneling dielectric layer and the substrate to form trenches therein together without previously patterning the first conductive layer and the tunneling dielectric layer. Hsieh actually does not teach this feature of the claimed invention. Furthermore, Hsieh particularly uses an additional defined sacrificial layer as a mask to form shallow trench isolations. This sacrificial layer 58 is crucial for the teaching of Hsieh and can not be omitted.

Hsieh further teaches that an HDPCVD process is subsequently

performed to deposit an HDP oxide layer 62 on the surface of the semiconductor wafer 50 filling the STI pattern 64. A planarization technique, such as a chemical mechanical polishing (CMP) process, is applied to removing the HDP oxide layer 62 over the sacrificial layer 58 using the sacrificial layer 58 as a stop layer to obtain a planar topography. Here further shows that the sacrificial layer 58 is crucial for the teaching of Hsieh and can not be omitted since Hsieh particularly points out that the sacrificial layer 58 is used as a stop layer in the CMP process to obtain a planar topography.

Thereafter, an HDP oxide etch back process is performed. A polysilicon layer 66 is then deposited over the sacrificial layer 58, the polysilicon layer 56 and the HDP oxide layer 62 or the surface of the semiconductor wafer 50. A polysilicon etch back process is performed next to remove the polysilicon layer 66 down to the surface of the HDP oxide layer 62. The remaining portions of the polysilicon layer 66 on the exposed vertical walls of the polysilicon layer 56 and sacrificial layer 58 form polysilicon spacers 68. The sacrificial layer 58 directly increases the height of the polysilicon spacers 68 and once again it further shows that the sacrificial layer 58 is crucial for the teaching of Hsieh and can not be omitted.

The sacrificial layer 58 is then completely removed which is not necessary in the claimed invention using wet chemistry, such as hot phosphoric acid. As shown in FIG. 13 of Hsieh, the polysilicon spacers 68 extend upward and over the top surface of the polysilicon layer 56 which is a crucial feature of the teaching of Hsieh.

Another strong evidences which shows that the sacrificial layer 58 is crucial for the teaching of Hsieh and can not be omitted are the

thicknesses of the tunneling oxide layer 54, the polysilicon layer 56, the sacrificial layer 58, the removed HDP oxide layer and the polysilicon layer 66. According to the teaching of Hsieh, the thickness of the tunneling oxide layer 54 is between 40 to 200 angstroms, the thickness of the polysilicon layer 56 is about 2000 angstroms, the thickness of the sacrificial layer 58 is about 1000 to 2000 angstroms, the predetermined thickness of the removed HDP oxide layer is about 2000 to 3500 angstroms, and the thickness of the polysilicon layer 66 is about 1000 angstroms. Hseih discloses that this removed HDP oxide layer is removed by an etch back process after a CMP process. That is, the top surfaces of the sacrificial layer 58 and the HDP oxide layer 62 are planar. If the sacrificial layer 58 is omitted, the total thickness of the tunneling oxide layer 54 and the polysilicon layer 56 is 2040(40+2000) to 2200(200+2000) angstroms. However, the predetermined thickness of the removed HDP oxide layer is about 2000 to 3500 angstroms which means that the top surface of remained HDP oxide layer is only 40 angstroms higher than the surface of the substrate 52 or the top surface of remained HDP oxide layer is 1300 angstroms lower than the surface of the substrate 52. That is, the top surface of remained HDP oxide layer is at a level between 40 angstroms above and 1300 angstroms below the surface of the substrate 52. More particularly, if the top surface of remained HDP oxide layer is in this range resulting from the omission of the sacrificial layer 58, then this proposed modification would violate the intended purposes of the teaching of Hseih since Hseih wants that the surface of the remaining HDP oxide layer 62 approximately flush with a line at half the thickness of the polysilicon layer 56(see col. 4, lines 13-16). It is quite clear that the top surface of remaining HDP oxide layer 62 is definitely below the line at half the thickness of the polysilicon layer 56 if the sacrificial layer 58 is omitted. Therefore, the sacrificial layer 58 is a crucial element in the method of Hseih and the omission of

the sacrificial layer 58 would violate the intended purposes of the teaching of Hseih so that Hseih actually discloses a different method comparing to the claimed invention. That is, the cited reference Hseih must be considered in its entirety according to MPEP § 2141.02. Therefore, one with ordinary skill in the art could not anticipate the claimed invention by the teaching of Hseih.

Claims 7-12 are rejected under 35 U.S.C. § 102(e) as being anticipated by Hsieh (US 6,326,263).

This rejection is traversed because Hsieh actually fails to teach every element of the claimed invention according to MPEP §2131 and the cited reference Hseih must be considered in its entirety according to MPEP § 2141.02. Contrary to the teaching of Hsieh, the claimed invention patterns the first conductive layer, the tunneling dielectric layer and the substrate to form trenches therein together without previously patterning the first conductive layer and the tunneling dielectric layer. Hsieh actually does not teach this feature of the claimed invention. Furthermore, Hsieh particularly uses an additional defined sacrificial layer as a mask to form shallow trench isolations. This sacrificial layer 58 is crucial for the teaching of Hsieh and can not be omitted. Hsieh particularly uses an additional defined sacrificial layer as a mask to form shallow trench isolations so that this sacrificial layer 58 is crucial for the teaching of Hsieh and can not be omitted. The sacrificial layer 58 directly increases the height of the polysilicon spacers 68 and once again it further shows that the sacrificial layer 58 is crucial for the teaching of Hsieh and can not be omitted. According to the teaching of Hseih, the top surface of remaining HDP oxide layer 62 is definitely below the line at half the thickness of the polysilicon layer 56 if the sacrificial layer 58 is omitted. Therefore, the sacrificial layer 58 is a

crucial element in the method of Hseih and the omission of the sacrificial layer 58 would violate the intended purposes of the teaching of Hseih so that Hseih actually discloses a different method comparing to the claimed invention. Therefore, one with ordinary skill in the art could not anticipate the claimed invention by the teaching of Hseih.

Rejection of Claim 2 Under 35 U.S.C. §103(a)

Claim 2 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hseih in view of Lee (US 6,380,032).

Applicants respectfully traverse this rejection since Lee does not teach the element which Hseih fails to disclose and the forming process of the floating gate 140, 220 of Lee is actually the same with that of the prior art of Hseih which Hseih wants to replace. The combination of Hseih and Lee not only fails to teach that the first conductive layer, the tunneling dielectric layer and the substrate are patterned together to form trenches, but also violates the intended purposes of the teaching of Hseih since Hseih wants the floating gate to be formed by a self-aligned process and the STI to be formed by an etch back process while Lee discloses the prior art of Hseih which would cause misalignment when defining the floating gate and insufficient coupling ratio. Thus Hseih and Lee are actually uncombinable and even Hseih and Lee are combined the combination of Hseih and Lee still fails to teach every element of the claimed invention. therefore, the teachings of Hseih and Lee are insufficient to render the claimed invention unpatentable.

Conclusion

In light of the above remarks to the claims, Applicant contends that Claims 1-12 are patentable thereover. The claims are in condition for favorable consideration and Applicant respectfully requests that a timely Notice of Allowance be issued in this case.